86 Family Interview Questions And Answers Guide.

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86 Family Job Interview Preparation Guide.

Question # 1

Tell me How do you detect if two 8-bit signals are same?

Answer:-

By using XNOR gate if the signals are same then only the output will be one otherwise not.

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Question # 2

Design any FSM in VHDL or Verilog?

Answer:-

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL; ----using all functions of
specific package---
ENTITY tollbooth2 IS
   PORT (Clock,car_s,RE : IN STD_LOGIC;
         coin_s         : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
         r_light,g_light,alarm : OUT STD_LOGIC);
END tollbooth2;
ARCHITECTURE Behav OF tollbooth2 IS
TYPE state_type IS
(NO_CAR,GOTZERO,GOTFIV,GOTTEN,GOTFIF,GOTTWEN,CAR_PAID,CHEATE
D);
------GOTZERO = PAID $0.00---------
------GOTFIV = PAID $0.05----------
------GOTTEN = PAID $0.10----------
------GOTFIF = PAID $0.15----------
------GOTTWEN = PAID $0.20---------
SIGNAL present_state,next_state : state_type;
BEGIN
-----Next state is identified using present state,car &
coin sensors------
    PROCESS(present_state,car_s,coin_s)
     BEGIN

     CASE present_state IS
      WHEN NO_CAR =>
       IF (car_s = '1') THEN
          next_state <= GOTZERO;
        ELSE
          next_state <= NO_CAR;
       END IF;
     WHEN GOTZERO =>
      IF (car_s ='0') THEN
      next_state <= CHEATED;
        ELSIF (coin_s = "00") THEN
        next_state <= GOTZERO;
        ELSIF (coin_s = "01") THEN
         next_state <= GOTFIV;
        ELSIF (coin_s ="10") THEN
         next_state <= GOTTEN;
      END IF;
    WHEN GOTFIV=>
     IF (car_s ='0') THEN
      next_state <= CHEATED;
       ELSIF (coin_s = "00") THEN
       next_state <= GOTFIV;
```

```
      ELSIF (coin_s = "01") THEN
       next_state <= GOTTEN;
      ELSIF (coin_s <= "10") THEN
       next_state <= GOTFIV;
   END IF;
  WHEN GOTTEN =>
   IF (car_s ='0') THEN
     next_state <= CHEATED;
     ELSIF (coin_s ="00") THEN
     next_state <= GOTTEN;

     ELSIF (coin_s="01") THEN
       next_state <= GOTFIV;
     ELSIF (coin_s="10") THEN
       next_state <= GOTTWEN;
   END IF;
  WHEN GOTFIF =>
   IF (car_s ='0') THEN
      next_state <= CHEATED;
      ELSIF (coin_s = "00") THEN
      next_state <= GOTFIF;

      ELSIF (coin_s ="01") THEN
         next_state <= GOTTWEN;
      ELSIF (coin_s = "10") THEN
         next_state <= GOTTWEN;
    END IF;
  WHEN GOTTWEN =>
     next_state <= CAR_PAID;
  WHEN CAR_PAID =>
   IF (car_s = '0') THEN
     next_state <= NO_CAR;
    ELSE
     next_state<= CAR_PAID;
  END IF;

 WHEN CHEATED =>
    IF (car_s = '1') THEN
    next_state <= GOTZERO;
    ELSE
    next_state <= CHEATED;
 END IF;
END CASE;
END PROCESS;-----End of Process 1
-------PROCESS 2 for STATE REGISTER CLOCKING--------
PROCESS(Clock,RE)
 BEGIN
  IF RE = '1' THEN
     present_state <= GOTZERO;
----When the clock changes from low to high,the state of
the system
----stored in next_state becomes the present state-----
      ELSIF Clock'EVENT AND Clock ='1' THEN
     present_state <= next_state;
  END IF;
 END PROCESS;-----End of Process 2-------
------------------------------------------------------------
-----Conditional signal assignment statements----------
r_light <= '0' WHEN present_state = CAR_PAID ELSE '1';
g_light <= '1' WHEN present_state = CAR_PAID ELSE '0';
alarm <= '1' WHEN present_state = CHEATED ELSE '0';
END Behav;
```

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Question # 3

Explain RC circuit?s charging and discharging?

Answer:-

Charging a Capacitor:
The voltage across the capacitor is not instantaneously equal to that of the voltage across the battery when the switch is closed. The voltage on the capacitor builds up as more and more charges flows onto the capacitor until the battery is no longer able to "push" any more charge onto the capacitor, at which point the capacitor becomes fully charged.
The initial flow of charges from the battery to the capacitor means that there is a current flowing through the system until the capacitor is charged. This current flow decays exponentially from some initial value to zero.

DisCharging a Capacitor:
Switch remains open and voltage across capaciotr decreses
untill it reaches zero.

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Question # 4

What are tri-state devices and why they are essential in a bus oriented system?

Answer:-

In a multiplexed bus system, many devices are connected to
a common bus. If 2 or more devices attempt to use the bus
at the same time , then data will be lost. Thus only one
one device must be allowed to use the bus at a time. O e
method is to connect the devices through tri-state
devices , which when disabled will effectively discoonect
devices from the bus.

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Question # 5

What is a program counter? What is its use?

Answer:-

It is a 16 bit special function register in the 8085
microprocessor.It keeps track of the the next memory
adderess of the instruction that is to be executed once the
execution of the current instruction is completed.In other
words, it holds the address of the memory location of the
next instruction when the current instruction is executed by
the microprocessor.

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Question # 6

How to detect a sequence of "1101" arriving serially from a signal line?

Answer:-

Use 4 D-bascules connected in serial, all synchronized with
the same CLK. Then connect all 4 outputs, & 2nd output must
reverse, of the D-bascule to an AND logic. The output of
the AND logic sould have '1' when it detectes "1101". This
technic oftenly use for glitch detection in the signal.

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Question # 7

Suppose you have a combinational circuit between two registers driven by a clock. What will you do if the delay of the combinational circuit is greater than your clock signal?

Answer:-

Put even number of not gates between clocks of reg A and
Reg B. The not gates will introduce delay between clock of
reg A and reg B.

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Question # 8

Explain the working of a binary counter?

Answer:-

in binary counter the flip flop of lowest order position is
complemented with every pulse.this means that JK input
position must me maintained with logic one

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Question # 9

Where can we find the sample ASSEMBLY LANGUAGE programs?

Answer:-

write a c code.
and generate the assembly for it using
cc -S xyz.c -o xyz.S
xyz.Swill contain assembly for your c code with instructions
of the processor of your computer/hardware

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Question # 10

Please give a circuit to divide frequency of clock cycle by two?

Answer:-

a T flip flop act as a frequency divider

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Question # 11

Give truth table for a Half Adder, Give a gate level implementation of the same?

Answer:-

x y c s
0 0 0 0
0 1 0 1
1 0 0 1
1 1 1 0

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Question # 12

What is ALE? Explain the functions of ALE in 8085?

Answer:-

address latch enable...in the case of microcontroller (8051)
& microprocessor 8085 the data line & low order 8 bit
address lines are multiplexed.in order to geting address
from this line we uses a latch.ALE is the line connected to
this latch saying that the take the address from the line.
NB: this is used only when we connecting our micro
controller to external mem.

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Question # 13

Explain two ways of converting a two input NAND gate to an inverter?

Answer:-

1)Short both I/Ps of NAND gate & use the gate as an
inverter.
2)Connect any one of the two I/Ps to VCC & use the
remaining I/P & use the gate as an inverter.

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Question # 14

Write an assembly code which can call function in a loop with al value from 0 to 9?

Answer:-

```
mov ro,#10h
here:
      acall fun
      inc   a1
      djnz  ro,here
```

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Question # 15

Explain What is the difference detween ISR & function call?

Answer:-

in isr there is no return value but in function call there
is return value

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Question # 16

What are set up time & hold time constraints What do they signify Which one is critical for estimating maximum clock frequency of a circuit?

Answer:-

Set up time constraint signifies how late the input signal
can arrive before the active edge of the flip-flop. Smaller
the set up time, the better.
Hold time on the other hand signifies how long the value at
the input needs to be held stable after the the active edge.
Again the smaller the hold time, the better.
For estimating maximum clock frequency, set up time is critical.

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Question # 17

Design a divide-by-3 sequential circuit with 50% duty circle now?

Answer:-

```
incoming clock by  ODD value as assigned  in genric
CLK_DIV_BY generic with
50% duty cycle
-------------------------------------------------------------
----------

library IEEE;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.std_logic_unsigned.all;
entity FDIV is

     generic(
                CLK_DIV_BY : INTEGER :=15; --Give the
odd value with which you want to divide the clock i.e.
3,5,7,9
                COUNTVALUE : INTEGER :=4 --Give the bit
count of division ratio value.Ex upto 3= 2 bits; 5 to 7 =
3; 9 to 15 = 4 and so on..
                 );
           port(
               CLK : in std_logic;
               CLR : in std_logic;
               DIV: out std_logic
               );
end FDIV;
-------------------------------------------------------
Architecture beh of FDIV is
signal DIV_pos, DIV_neg :std_logic;
signal posedgecounter  :std_logic_vector((COUNTVALUE - 1)
downto 0);
signal negedgecounter,test  :std_logic_vector((COUNTVALUE -
1) downto 0);
begin
-----------------------------
PROCESS(CLK,CLR)
begin
 IF ( CLR = '0') THEN
    posedgecounter <= (others =>'0');
 ELSIF RISING_EDGE(CLK) THEN
    posedgecounter  <= posedgecounter + 1;
    if  posedgecounter = conv_std_logic_vector((CLK_DIV_BY -
 1),(COUNTVALUE)) then
      posedgecounter <= (others =>'0');
    end if;
   if posedgecounter <= conv_std_logic_vector(((CLK_DIV_BY -
1)/2),(COUNTVALUE)) then
        DIV_pos <= '1';
    else
        DIV_pos <= '0';
   end if;
 END IF;
END PROCESS;
-----------------------------
PROCESS(CLK,CLR)
begin
 IF ( CLR = '0') THEN
   negedgecounter <= (others =>'0');
 ELSIF FALLING_EDGE(CLK) THEN
    negedgecounter  <= negedgecounter + 1;
    if negedgecounter = conv_std_logic_vector((CLK_DIV_BY -
1),(COUNTVALUE))  then
      negedgecounter <= (others =>'0');
    end if;
    if negedgecounter <= conv_std_logic_vector
((((CLK_DIV_BY -1)/2),(COUNTVALUE)) then
       DIV_neg <= '1';
    else
       DIV_neg <= '0';
    end if;
 END IF;
END PROCESS;
---------------------------------------
DIV<= DIV_pos and DIV_neg;
---------------------------------------
end beh;
```

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Question # 18

Design a Transmission Gate based XOR. Now, how do you convert it to XNOR?

Answer:-

put one bubble in front of xor gate....

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Question # 19

Explain an interrupt?

Answer:-

used to interrupt cpu ,s normal execution routine and to get
its attention .mostly generated by an external devices,
timers,countres...etc

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Question # 20

What do you mean by embedded system?

Answer:-

it is a combination of hardware and software to perform
desired task

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Question # 21

Which line will be activated when an output device require attention from CPU?

Answer:-

INTR (interrupt request)

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Question # 22

What are different Adder circuits you studied?

Answer:-

Half Adder (for addition of two bits)
Full Adder (for addition of three bits)
Carry propagate adder
Carry save adder
Carry look ahead adder

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Question # 23

Explain Transmission Gate-based D-Latch?

Answer:-

The Transmission-Gate input is connected to the D_LATCH
data input (D), the control input to the Transmission-Gate
is connected to the D_LATCH enable input (EN) and the
Transmission-Gate output is the D_LATCH output (Q)

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